IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., Plaintiff, v. GOOGLE LLC, Defendant.	)	Case No. 6:19-cv-00515-ADA
SOLAS OLED LTD., Plaintiff, v. APPLE INC., Defendant.	)	Case No. 6:19-cv-00537-ADA
SOLAS OLED LTD., Plaintiff, v. HP INC., Defendant.	)	Case No. 6:19-cv-00631-ADA

DEFENDANTS' AND INTERVENTOR'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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AA06	Solas Notice Of Agreement On Previously Disputed Claim Construction Terms, *Solas OLED Ltd. v. Samsung Display Co.*, 2:19-cv-00152-JRG, Dkt. 98 (E.D. Tex., April 15, 2020)
DD07	Steven M. Kaplan, Wiley Electrical and Electronics Engineering Dictionary 237 (John Wiley & Sons, Inc., 2004)
DD08	Collins Dictionary Electronics 139 (HarperCollins, 2007)
DD09	Erin McKean, The New Oxford American Dictionary 545 (Oxford University Press, 2nd ed. 2005)

Solas's opening brief ("Solas Open. Br.") takes a flawed approach to claim construction. For many terms, instead of addressing the intrinsic evidence, Solas's argument consists solely of repeated refrains that its construction reflects the plain and ordinary meaning and that Solas is not aware of any redefinition or disclaimer. But many of the disputed terms are phrases specially coined in the patents and have no ordinary meaning outside of the patents. Worse, to support its understanding of the ordinary meaning, Solas cites dictionary definitions rather than the intrinsic evidence, taking the very approach that the Federal Circuit rejected en banc in *Phillips*. *E.g.*, *Phillips v. AWH Corp.*, 415 F.3d 1303, 1320-21 (Fed. Cir. 2005) (en banc). Precedent is clear that the ordinary meaning "of a claim term is its meaning to the ordinary artisan after reading the entire patent" and not "in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history." *Id*. at 1313, 1321.

Rather than address the intrinsic record, Solas spends most of its opening brief attacking Defendants' constructions. But Solas's attacks ignore the true, substantive differences between the parties' proposals, favoring instead superficial objections that apply to many of Solas's own proposals. And for several terms, Solas's cursory arguments are undermined by the declaration of its own expert, Mr. Richard Flasck ("Flasck Decl.").

I. U.S. Patent No. 7,446,338 ("'338 Patent")

A. "transistor array substrate" (claim 1)

Plaintiff's Proposal	Defendants' Proposal
"layered structure upon which or within which a transistor array is fabricated"	"a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors"

Solas's arguments against Defendants' proposal mirror the arguments Solas originally made in its briefing and oral argument at the *Markman* hearing in *Solas OLED Ltd. v. Samsung Display Co.*, 2:19-cv-00152-JRG (E.D. Tex). Yet unmentioned by Solas is that shortly after it

made these arguments in the Eastern District of Texas, Solas explicitly informed the Court that it changed its position, and submitted a "Notice of Agreement" *expressly agreeing to Defendants' proposed construction of "transistor array substrate" as the proper construction for that term in the '338 patent*. Ex. AA06 (*Solas OLED Ltd. v. Samsung Display Co.*., 2:19-cv-00152-JRG, Dkt. 98 (E.D. Tex., April 15, 2020)). Solas then represented to the PTAB, in responding to Samsung Display Co.'s IPR petition on the '338 patent, that Solas had *agreed* to the Defendants' proposed construction of "transistor array substrate" in the '338 Patent. Defs. Open. Br., Ex. AA05 at 27–28. Judge Gilstrap ultimately did not accept Solas's "late-breaking Notice of Agreement," which Solas did not submit to the Court until two days before the Court issued its claim construction opinion and Order. But Solas's representations to the PTAB are new intrinsic evidence supporting Defendants' construction. Thus, there is a crucial difference between this proceeding and the Eastern District of Texas matter, and important new evidence that supports Defendants' proposed construction.

Solas is hard-pressed to argue that Defendants' construction is inappropriate, given that Solas informed the Eastern District of Texas, and the PTAB, that Solas ***agrees*** to that construction. Moreover, Solas offers no sound reason for turning its back on its prior agreement, and advancing a position inconsistent with what it urged before the PTAB and represented to Judge Gilstrap was an appropriate construction of the '338 Patent. Indeed, it is ironic that Solas devotes much of its brief to chiding Defendants for purportedly seeking a "do-over" when Defendants are simply proposing the same construction that Solas itself agreed to and represented to the PTAB that it was agreeing to.

As noted in Defendants' opening brief ("Defs. Open. Br.," Dkt. 73 in the Google action, No. 6:19-cv-00515-ADA), the Eastern District found that the *specification's* references to a

transistor array substrate containing an array of transistors did not justify including the requirement. *See* Defs. Open. Br., Ex. AA02 at 14. Defendants respectfully submit that the *claim language* of the '338 Patent is decisive and supports Defendants' construction, as outlined in Defendants' opening brief. Defs. Open. Br. at 2–5. None of Solas's arguments to the contrary are persuasive, and, in fact, many were expressly rejected as part of Judge Gilstrap's Order.

Defendants' proposed construction of the term "transistor array substrate" is the meaning given to that term in the '338 Patent. While Solas cites to dictionary definitions of "substrate" in support of its construction, Solas does not cite to a single dictionary definition of the term at issue, "transistor array substrate." Solas Open. Br. at 9. That is because, unlike the term "substrate," the term "transistor array substrate" has no ordinary and customary meaning in the art, as recognized by Judge Gilstrap and Solas's expert. Defs. Open. Br., Ex. AA02 (Claim Construction Memorandum and Order) at 10 ("Plaintiff's expert has acknowledged that the term 'transistor array substrate' does not have a specific, well-established meaning in the relevant art."). In fact, the '338 Patent explicitly describes an "insulating substrate 2"—the substrate described in Solas's dictionary definitions—as being only one of numerous different layers that make up the '338 Patent's "transistor array substrate." '338 at 10:42–47 ("The layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50."). While dictionaries may assist the Court in determining the meaning of particular terminology, extrinsic evidence like dictionaries is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips*, 415 F.3d at 1317 (internal quotation marks omitted). Here, the claim language is determinative. The "transistor array substrate" must "comprise a plurality of transistors," and must consist of the layers formed under the pixel

electrodes, given that the pixel electrodes are "arrayed . . . *on the surface transistor array substrate*." '338 at 24:15–25 (Emphasis added).

Solas criticizes Defendants for relying on, in addition to the claim language, the embodiment shown in Figure 6. But the Figure 6 embodiment is consistent with the claim language described above, and is the figure that the patent used to describe the structure of the claimed inventions. Significantly, the specification does not disclose any "transistor array substrate" other than the "transistor array substrate 50" shown in Figure 6. Consistent with Defendants' construction, the '338 Patent states that "[t]he layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50." '338 at 10:45–47.

Solas also errs in asserting that Defendants' construction is somehow inconsistent with the specification in defining the top of the "transistor array substrate" in terms of its relationship to the pixel electrodes, as opposed to "insulating line 61." Solas Open. Br. at 10–11. There is no inconsistency. Defendants' construction comes directly from the claim language, which, as described above, expressly states that the pixel electrodes are formed on the surface of the transistor array substrate. *See also* '338 at 11:50–52 ("The plurality of sub-pixel electrodes 20*a* are arrayed in a matrix on the upper surface of the transistor array substrate 50."). The claim does not require the insulating layer, but specifies that the pixel electrodes are on the surface of the transistor array substrate. The fact that another structure such as insulating line 61 may *also* be on a portion of the transistor array substrate does not detract in any way from the fact that the pixel electrodes are on the surface of the transistor array substrate. Notably, when Solas made the same flawed argument in the Eastern District, Judge Gilstrap found that "Plaintiff fail[ed] to justify precluding multiple structures from being formed on a transistor array substrate." Defs. Open. Br., Ex. AA02 (Claim Construction Memorandum and Order) at 12–13.

Similarly, as it did in the Eastern District, Solas erroneously argues that Defendants' construction would exclude a "top emission type" embodiment of the '338 Patent from the claims. Solas Open. Br. at 11. But as Judge Gilstrap concluded, Solas's argument has no merit: "Defendants' proposed construction is . . . consistent with both the 'bottom emission type' and the 'top emission type.'" Defs. Open. Br., Ex. AA02 (Claim Construction Memorandum and Order) at 12. "If a reflecting film is thus present, then under Defendants' proposed construction the reflecting film would be part of the 'transistor array substrate' because the reflecting film would be the layer upon which the pixel electrodes are formed." *Id.*

Thus, consistent with the intrinsic evidence, as well as Solas's prior agreement, "transistor array substrate" should be construed as "a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors"[1]

B. "project from a surface of the transistor array substrate" (claim 1)

Plaintiff's Proposal	**Defendants' Proposal**
"extend from an external surface of the transistor array substrate"[2]	"extend above the upper surface of the transistor array substrate"

The specification makes clear that the interconnections "project upward from the upper transistor array substrate, as Defendants propose. The '338 Patent explains that "[t]he common interconnection 91 is . . . formed to . . . *project upward from the surface* of the planarization film

[1] To the extent Solas takes issue with Defendants' construction including the term "insulating layer," Solas Open. Br. at 9, to narrow the dispute, Defendants would be willing to alter their construction to "a layered structure composed of a bottom *substrate* layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors."

[2] Solas proposed this construction in its exchange of proposed claim constructions and included it in the box at the beginning of the section for this term in its opening brief. *See* Solas Open. Br. at 12. However, in its brief, Solas urges the Court to "adopt the constructions that Judge Gilstrap held were correct" i.e. "extend beyond an outer surface of the transistor array substrate. *See id.*, Defs. Open. Br., Ex. AA02 (Claim Construction Memorandum and Order) at 12–13 at 18.

33." '338 at 10:54-58 (emphasis added). The specification then further explains that "select interconnection 89 and feed interconnection 90 *project upward from the upper surface* of the planarization film 33." *Id*. at 11:36-41 (emphasis added). As the patent explains, the "surface" or "upper surface" of the planarization film 33 is the upper surface of the transistor array substrate. *See, e.g., id*. at 10:49-51 ("the surface of the planarization film 33, ***i.e***., the surface of the transistor array substrate 50") (emphasis added); 11:50-52 ("the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate 50"). Figure 6 (annotated below) confirms this, showing the interconnections (89, 90, and 91 shown in red) all extend above the upper surface of the planarization film (33 shown in yellow) of the transistor array substrate 50:

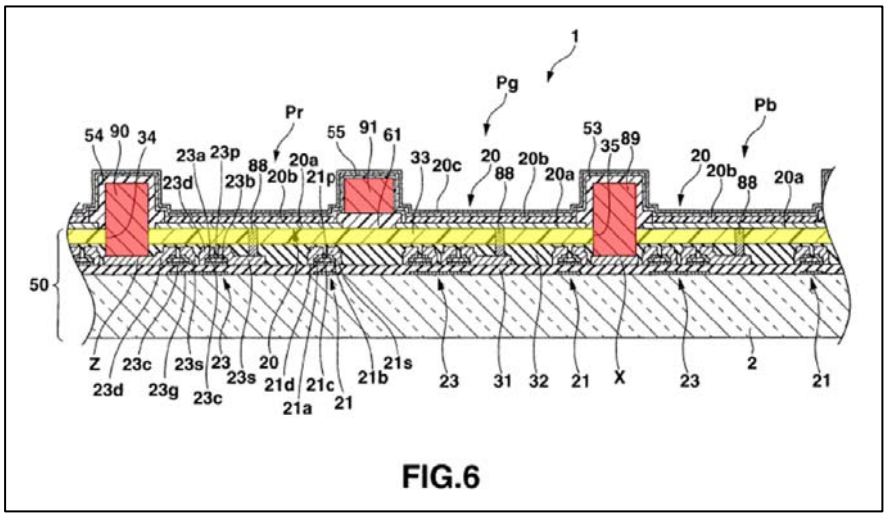


FIG.6

While Judge Gilstrap largely adopted Defendants' construction in the Eastern District of Texas litigation, he declined to include the "upper" portion of Defendants' construction, stating that the term "upper" "lacks sufficiently clear meaning in the context of a 'display panel' as claimed in . . . Claim 1." Defs. Open. Br., Ex. AA02 (Claim Construction Memorandum and Order) at 18. Defendants respectfully disagree in that their proposed construction uses the same language that the patent uses, which would be understood by persons skilled in the art and would assist the jury by clarifying how the interconnections project from the transistor array substrate.

Solas's briefing shows why the inclusion of "upper" in the construction is necessary. Solas argues the specification's references to interconnections that "project upward from the *upper surface* of the planarization film" and interconnections that "project upward from the *surface* of the planarization film" shows that "the specification does not always specify that interconnections project from the upper surface." Dkt. 74 at 12 (emphases added). Solas's argument assumes that the interconnections, which the specification states are formed to "project upward," can project upward from a surface other than the upper surface of the transistor array substrate. But this is contradicted by the very construction that Solas advances, which requires the interconnections to "extend beyond an outer surface of the transistor array substrate," as an interconnection cannot project upward and extend beyond any outer surface other than the upper surface.

Further, if the interconnections did not extend beyond the upper surface of the transistor array substrate, they would not fulfill a stated purpose of the projecting interconnections, which the '338 Patent repeatedly explains is to "serve as partition walls to prevent leakage of an organic compound-containing solution." *See* '338 at 6:24-30, 6:38-42; *see also Phillips*, 415 F.3d at 1316 ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction."). The interconnections must extend past the upper surface of the transistor array substrate to serve as leakage-preventing partition walls, as the specification explains: "[t]he thick select interconnection 89, feed interconnection 90, and common interconnection 91 *whose tops are much higher than that of the insulating line 61* are formed between the sub-pixel electrodes 20a adjacent in the vertical direction to project [sic] respect to the surface of the transistor array substrate 50. Hence, the organic compound-containing solution applied to a sub-pixel electrode 20a is prevented from leaking to the sub-pixel electrode 20a adjacent in the vertical direction." *Id*. at 12:62-13:3 (emphases added).

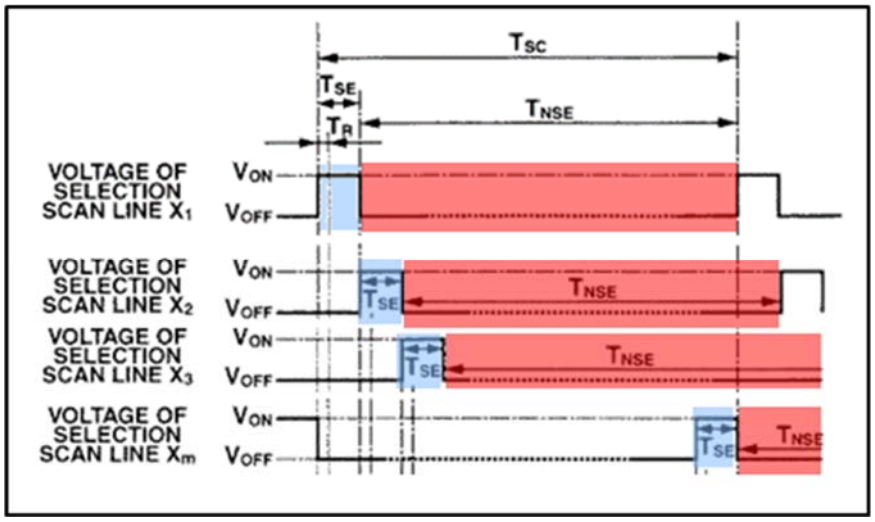
As seen in Fig. 6 (annotated above), insulating line 61 is located along the upper surface of the transistor array substrate. The interconnections extend above the upper surface of the transistor array substrate, as Defendants propose, to perform this function, and could not do so if they projected from the other external surfaces (i.e., the side or bottom surfaces).

II. U.S. Patent No. 7,499,042 ("'042 Patent")

A. "selection period" (Claim 1)

Solas's Proposal	HP's Proposal
"time period during which a plurality of pixel circuits is selected"	"time duration in which a selected selection scan line is kept active"

Solas's opening brief shows that its attempt to define "selection period" without reference to a "selection scan line" is contrived, contrary to the specification's express definition, and leads to absurd results. Conversely, Solas raises no substantive disputes with HP's construction. Solas, for example, does not dispute that a "selection period" refers to the time a "selection scan line" is active, or that the "selection scan line" must be kept active during this entire period. Instead, Solas nitpicks over whether the words "duration" and "active" are ambiguous in HP's construction.



As described in HP's opening brief and illustrated in Figure 4 (annotated), the specification expressly defines "selection period" as the time when one corresponding "selection scan line" is selected and kept active (blue), while defining other inactive times as a "non-selection period" (red) for that "selection scan line". Defs. Open. Br. at 9-11; '042 at 9:13-32, 9:49-57. At any given time, only one "selection scan line" for one row of pixels in a display panel is selected.

Solas acknowledges that the meaning of "selection period" is tied to a "selection scan line." Solas Open. Br. at 17-18. In particular, Solas quotes the same, aforementioned definition of "selection period" from the specification: "a period in which the selection scan driver 5 … selects the *selection scan line* Xi in the ith row *is called a selection period* TSE of the ith row." *Id.* at 17 (citing '042 at 9:22-27). As Solas further acknowledges, each "selection scan line" is connected to one associated *row* of pixel circuits. *Id.* ("In the second transistor 22 of *each of the pixel circuits Di,1 to Di,n in the ith row*, a gate 22 g *is connected to the selection scan line Xi in the ith row*."). Yet, Solas still proposes to construe "selection period" without reference to a "selection scan line" and to instead refer to any period when any "plurality of pixel circuits is selected."

Solas's proposal leads to the absurd outcome of allowing *any* time period to be a "selection period." This is because at any given time during the operation of a display panel, one row of pixel circuits in the display panel is selected, meaning that "a plurality of pixel circuits is selected" at all times. Put differently, Solas's proposal puts no bounds at all on a "selection period" because during the entire operation of a display panel, some "plurality of pixel circuits" is being selected.

HP's proposal poses no such substantive problems, and Solas identifies none. Instead, Solas objects to only the choice of wording in HP's construction. First, Solas claims that the term "kept active" is confusing and not used in the intrinsic evidence. Solas Open. Br. at 17-18. But Solas's own arguments undermine its claimed confusion. It recognizes that a "selection scan line" is "kept active" when "the "Von" voltage . . . is applied to the selection scan line." *Id.* at 18. Thus, Solas recognizes that "kept active" refers to when a "selection scan line" is in the "ON" state.[3] Critically, Solas presents no dispute to the key, substantive requirement in HP's

[3] HP is amenable to substituting "kept on" for "kept active" to address Solas's objection.

construction—namely that the "selection scan line" must be kept active (i.e., kept in the "ON" state) during the entire "selection period"; the "selection scan line" cannot be turned off.

Second, Solas argues that HP's construction uses redundant words because it states that the "selection scan line" is both "selected" and "kept active." Solas claims using both "selected" and "active" is unnecessary because both signify the same thing. *Id.* HP's construction, however, uses "*kept* active" to clarify that a selected "selection scan line" must *remain* active during the "selection period"—the selected selection scan line cannot be turned off or inactive during this time. Again, Solas presents no substantive dispute. Solas, for example, never suggests that a "selection scan line" can be turned off or inactive during a "selection period." Any such suggestion would contradict the specification, which uses a separate term, "non-selection period," to describe a time when a "selection scan line" is inactive. Defs. Open. Br. at 9-11; '042 at 9:49-57.

Third and finally, Solas argues that the term "duration" in HP's construction is inappropriate because "duration" refers to a time that has no specified beginning point T1 and end point T2. Solas Open. Br. at 18.[4] But HP's construction specifies *which* duration is discussed: the duration when "a selection scan line is kept active." This duration begins when a "selection scan line" is selected (T1), and ends when it is de-selected (T2). Solas's proposal, by contrast, places no limit on when a "selection period" can begin or end because it does not specify which "plurality of pixel circuits" is to be selected in this period as discussed above. Thus, whereas HP's construction gives "selection period" a meaning that comports fully with the intrinsic record, Solas proposal gives the term no meaning at all.

B. "sequentially selects said plurality of selection scan lines in each selection period" (Claim 1)

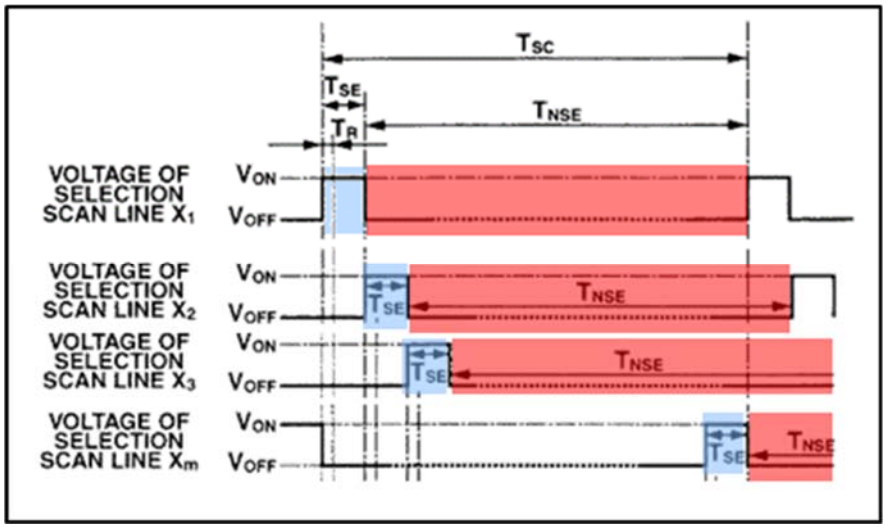
Solas's Proposal	HP's Proposal

[4] HP does not object to substitution of "period" for "duration," if deemed appropriate by the Court.

Plain and ordinary meaning	"selects said plurality of selection scan lines one per each of a plurality of non-overlapping selection periods"

As discussed in HP's opening brief, the 12-word phrase at issue here requires construction because it is a lengthy, technical phrase that lacks a plain and ordinary meaning outside the context of the '042 Patent. Defs. Open. Br. at 12-13. Hence, Solas is incorrect in asserting that the phrase's meaning can be derived from the dictionary definitions of just one of its twelve words, "sequentially." Solas Open. Br. at 19.

While incorrectly basing its construction on dictionary definitions of "sequentially," Solas disregards the intrinsic evidence, which confirms that "selection periods" for different "selection scan lines" must be "non-overlapping" in time, as detailed in HP's opening brief. Defs. Open. Br. at 12-13. To reiterate, the specification states that "*the selection periods* T_{SE} of the selection scan lines X_1 to X_m *do not overlap each other*." '042 at 9:29-31. This is because, as shown in Figure 4 (annotated), selection scan lines are selected one at a time; when an ON voltage is applied to one line, "*the selection scan driver 5 applies the OFF voltage* V_{OFF} *to the other selection scan lines.*" *Id.* at 9:26-29. Therefore the "selection period" T_{SE} for any one selection scan line (blue) occurs only during the non-selection periods T_{NSE} of the other selection scan lines (red).



Contrary to Solas's assertion, it is not the case that merely "an embodiment" discloses non-overlapping selection periods, while other embodiments do not. Solas Open. Br. at 19. Rather, *every* embodiment discloses non-overlapping selection periods while none discloses two or more

periods at overlapping times, as permitted under Solas's overbroad construction. On similar facts, in *Regents of University of Minnesota v. AGA Medical Corp*., the Federal Circuit construed "first and second disks" to create "separate[] . . . physically distinct disks" because the "specification never teaches an embodiment constructed as a single piece. Quite the opposite: every single embodiment disclosed in the . . . patent's drawings and its written description is made up of two separate disks." 717 F.3d 929, 935-36 (Fed. Cir. 2013). Likewise, in *ICU Medical, Inc. v. Alaris Medical Systems, Inc.*, the Federal Circuit construed "spike" to require a "pointed tip" because "[t]he specification never suggests that the spike can be anything other than pointed" and "each figure depicts the spike as elongated and pointed." 558 F.3d 1368, 1375-76 (Fed. Cir. 2009). Here, *every* relevant figure and passage of the specification discloses *non-overlapping* selection periods.

Solas's argument that the claim language "injects the possibility" of overlapping selection periods is incorrect for the same reason. Solas Open. Br. at 20. There is no embodiment where two (or more) selection scan lines can be selected at the same time, and Solas identifies none. Moreover, such an embodiment would be absurd and fundamentally at odds with the operation OLED circuits, which select only one selection scan line at a time. Defs. Open. Br. at 13-14.

C. "designating current" (Claim 1)

Solas's Proposal	HP's Proposal
Plain and ordinary meaning, *i.e.*, current designating a value corresponding to an image signal	"current corresponding to an image signal having a specified current value that is held constant"

Solas's claim that "'designating current' has a plain and ordinary meaning, understood by a POSITA" is unsupported and incorrect. Solas Open. Br. at 20. To the contrary, "designating current" is a term coined by the '042 Patent and its meaning must therefore be derived from the context of the intrinsic evidence. Here, the specification makes clear that a "designating current"

must have a ***constant*** current value[5] that corresponds to an image signal. Defs. Open. Br. at 14-15. Ignoring this express specification statement, Solas presents a slew of self-contradicting arguments that misinterpret other specification passages out of context.

First, Solas argues that "the specification never describes the designating current as held constant during the *first reset portion*" of a selection period and claims that ignoring this "reads out a preferred embodiment." Solas Open. Br. at 20-21. But Solas ignores that no "designating current" even exists during the "first reset portion" of a selection period.

As context, each selection period is divided into two sub-periods: (1) a first sub-period, known as the "*reset period* T_R of the ith row," where "the [data driving circuit] switches S_1 to S_n apply the reset voltage V_R to the current lines Y_1 to Y_n" ('042 at 13:10-30); and (2) a second sub-period where, a "designating current I_{DATA}" is applied "after the reset period T_R" (*id.* at 13:60-64). The data driver is only able to supply one of these signals—either reset voltage or designating current—at a time, as it contains a "switch Sj [that]. . . switches the state in which the current source driver 3 supplies the tone designating current I_{DATA} to the current line Y_j, and the state in which the reset voltage V_R is applied to the current line Y_j." *Id.* at 12:16-21. Claim 1 confirms and recites the same, stating "a data driving circuit which applies a *reset voltage . . . in a first part* of the selection period, and supplies a *designating current* . . . to said plurality of current lines *in a second part of the selection period* ***after applying the reset voltage*** *in the selection period*."

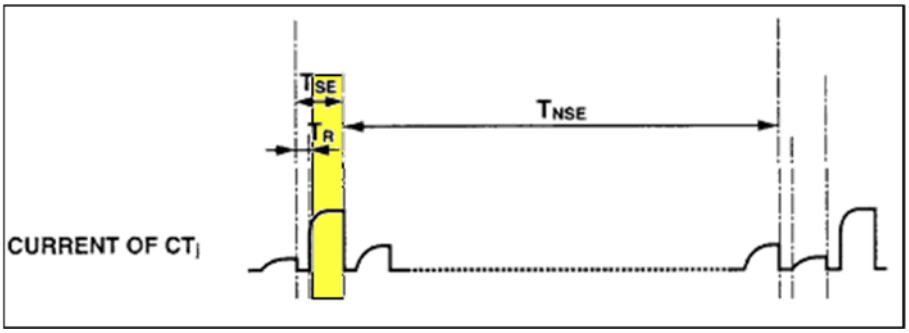
Because the data driving circuit only applies one of the "reset voltage" and "designating current" to the current line at any given time, no "designating current" can be supplied during the

[5] Solas at least agrees with HP that the "designating current" has or designates a "current value" corresponding to an image signal, not a "voltage value." *See* Solas Open. Br. at 21 ("the current source driver . . . generate[s] the tone designating current IDATA having *a current value corresponding to the image signal*."), 4-5 ("[T]he pixel circuit[] . . . stores a level of voltage converted in accordance with *the current value of the designating current*.").

"first reset portion" of the selection period. *Id.* at 11:41-12:34. Solas admits as much in describing the '042 Patent background, stating "[t]he driving circuit applies a reset voltage to the plurality of current lines *and then supplies a designating current.*" Solas Open. Br. at 4. What's more, Solas further admits that "the designating current is *held constant only during the second portion of the selection period*." *Id.* at 21. Thus, Solas agrees that the "designating current" is supplied in the "second portion" or sub-period and that it is held constant during that time frame.

Second, Solas quotes the statement: "[t]he current value of the tone designating current I_{DATA} decreases as the luminance tone lowers" to suggest that the "designating current" has a varying value. *Id.* at 21 (quoting '042 at 16:31-32). But this statement is unrelated to whether the "designating current" is held constant during a "selection period." Rather, it explains that the current value of the "designating current" correlates with luminance or brightness; so a given, constant current value causes a particular brightness or "luminance tone."

Third and finally, Solas points to Figure 9 (excerpted below) because it appears to show the "current of CT_j" rising in value during the second portion of the "selection period." Solas Open. Br. at 21. Solas claims that the "current of CT" is the *current* value of the designating current. *Id.* Solas misinterprets Figure 6 and omits critical context from the specification about what it actually depicts. The specification explains that Figure 9 shows the *voltage* applied during the flow of "current of CT_j"—not the *current* value of the designating current (or any other current for that matter). Specifically, the specification states: "As shown in FIGS. 7 and 9," "since the *voltage* [annotated yellow] *applied*



from the voltage supply line Zi in the ith row to the current terminals CT_1 to CT_n becomes steady, the *voltage having a level corresponding to the current value* of the tone designating current I_{DATA} . . . is held in the capacitor 24." *Id.* at 17:63-67, 18:19-44. The figure therefore shows a *voltage* value "becom[ing] steady" and says nothing about the current value of the "designating current." Meanwhile, this same passage confirms that the "current value is held constant" in this period, stating that "[u]ntil the end of the selection period TSE of the ith row [(yellow)], the current source driver 3 controls the current value of the tone designating current I_{DATA} supplied to the current lines Y_1 to Y_n such that *the current value is held constant* in accordance with the image signal." *Id*. at 17:63-18:18.

D. "current lines" (Claim 1)

Solas's Proposal	HP's Proposal
Plain and ordinary meaning, *i.e.*, conductive lines for carrying current	"conductive lines, each connected to a plurality of pixel circuits and carrying current"

The parties' briefs present contrasting approaches for how to define "current lines." Solas purports to base its construction on the "plain English" meaning of the individual words in the term, ignoring their context. HP's construction follows from the context of the '042 Patent and OLED technologies, where "current lines" connect to columns of pixel circuits, with each line connecting to one column. Defs. Open. Br. at 15-16. Figure 3 below depicts this arrangement, where an OLED display panel comprises a grid of pixels (blue) arranged across multiple rows and columns and each individual "current line" (red) connects to one column of pixel circuits. *Id*.

Solas fails to articulate any basis to reject that each "current line" connect to a "*plurality* of light emission drive circuits." Solas asserts that the requirement "is unsupported" and the "specification does not require" it. Solas Open. Br. at 22. Solas, however, cites nothing to support it assertion, and for good reason. In truth, *every* embodiment in the specification, including that of Figure 3, shows that each individual "current line" (red) connects to a column of multiple pixel circuits (blue). There is no contrary embodiment where each "current line" connects to *only one* single pixel circuit. *See Regents of Univ. of Minn.*, 717 F.3d at 935-36 (construing claims consistently with "every single embodiment" and because there was no contrary embodiment); *ICU Medical*, 558 F.3d at 1375-76 (same). Indeed, such a contrary embodiment would be absurd as it would require an OLED display panel having only one pixel or one row of pixels. Solas is thus incorrect in asserting that the "plain meaning" of "current lines" in the '042 Patent permits each line to connect to only one pixel.

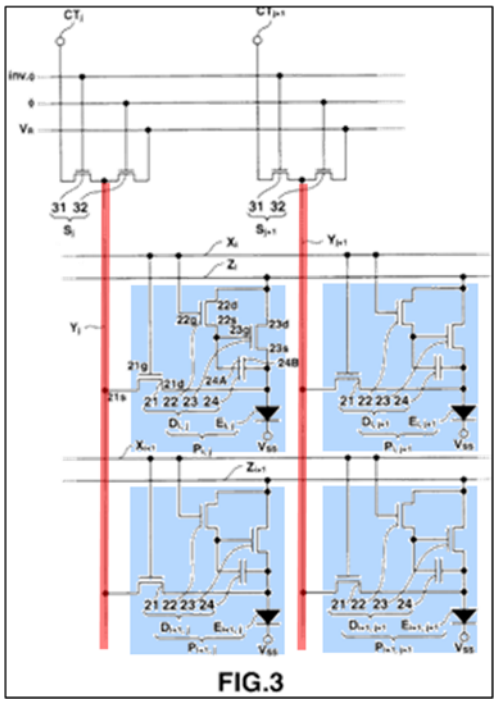


FIG.3

Solas is also incorrect in asserting that the use of "pixel circuits" in HP's construction is "superfluous" of surrounding claim language, which uses that phrase. Solas Open. Br. at 23. None of the surrounding claim language captures that "*each*" one of the "current lines" connects a plurality of pixel circuits, as clarified by HP's proposal. In any event, Solas cites no authority for rejecting a construction merely due to redundancy. To the contrary, while constructions that "render some portion of the claim language superfluous are disfavored," the "preference for giving meaning to all terms" is "not an inflexible rule that supersedes all other principles of claim

construction." *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016). In *SimpleAir*, the district court rejected a construction that would "render . . . additional language . . . redundant." *Id.* The Federal Circuit reversed because the preference to avoid redundancy is weak and "[c]laims must always be read in light of the specification" so "the construction [] stays true to the claim language and most naturally aligns with the patent's description of the invention." *Id.* at 429–30. Here, the specification evidence supporting HP's construction of "current lines" far outweighs any presumption against redundancy.

III. U.S. Patent No. 7,663,615 ("'615 Patent")

A. "the operation" (Claim 11)

Plaintiff's Proposal	HP's Proposal
Plain and ordinary meaning, not indefinite. Within the claim phrase "a drive voltage for making the light emission control section perform the operation," the term "the operation" refers to "generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element."	Indefinite

Solas concedes that "*the* operation" lacks any antecedent basis. But its construction, which actually includes two different proposals—(1) plain and ordinary meaning and (2) a 36-word phrase—does nothing to resolve the indefiniteness problem caused by the lack of antecedent basis. The two proposals in Solas's construction are also contradictory: the plain meaning of "the operation" is not the 36-word phrase and Solas does not argue otherwise.

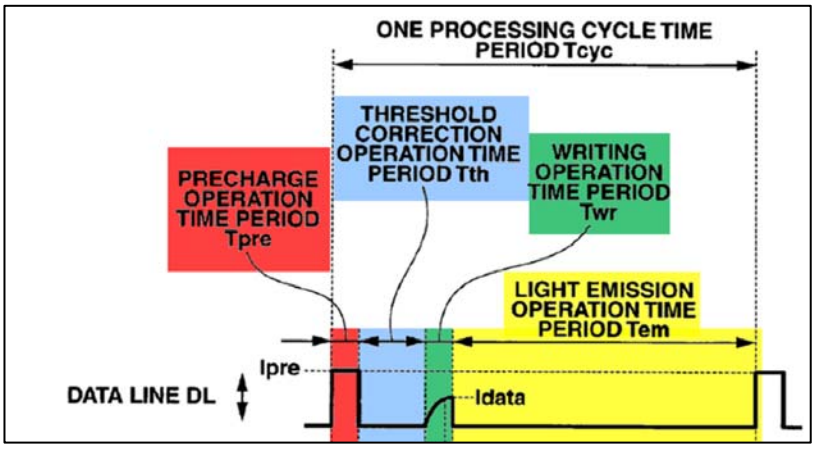
In defending the second 36-word proposal, Solas contends that Claim 11 is still definite because "the only reasonable reading of the claim" is that "the operation" refers to those 36 words. Solas Open. Br. at 24-25. To support its contention, Solas notes that "the operation" appears in relation to the phrase, "making the *light emission control section* perform *the operation*," and that its 36-word proposal is taken from functions that another element in Claim 11 attributes to the "light emission control section." *Id.* Solas then argues that "*the* operation" must refer to "*the*

operation of the *light emission control section*," rather than "just any operation mentioned in the specification." *Id.* Premised in Solas's argument is that the "light emission control section" performs only one kind of "operation" that is fully captured by its 36-word phrase and that corresponds to "the operation" in the claim.

The intrinsic evidence refutes the premises underlying Solas's argument. First, Solas's own 36-word proposal is not limited to only one kind of operation. It recites two different operations of: (1) "generating a light emission drive current . . ." and (2) "supplying the light emission drive current . . .."

Second, as HP's opening brief details and as Solas acknowledges, the specification identifies at least seven different "operations." Defs. Open. Br. at 18; Solas Open. Br. at 25. The specification does not describe any of those "operations" using Solas's 36-word proposal. Kanicki Resp. Decl. ¶9. And neither Claim 11 nor the specification refers to any of the functions that the other element of Claim 11 attributes to the "light emission control section" as "operations."

Third, the "light emission control section" is involved in performing *every* one of the several different "operations" in the specification—thus, no one "operation" that can be characterized as "*the* operation of the *light emission control section*." Kanicki Resp. Decl. ¶¶8-9. As the timing chart of Figure 2 (annotated) illustrates, the process of writing and displaying one pixel value is a cyclical process that requires performing four successive "operations" in each cycle: (1) a "precharge operation" (red); (2) a "threshold correction operation" (blue); (3) a



"writing operation" (green); and (4) a "light emission operation" (yellow). '615 at 18:37-19:9 (summarizing the four "operations"); Kanicki Resp. Decl. ¶¶10-17 (describing each "operation"). The parties have an agreed construction of "light emission control section" as "drive transistor" and in the specification, the "drive transistor" is element Tr13. Kanicki Resp. Decl. ¶11. The drive transistor Tr13 is turned on and performing an action, such as passing current or voltages, in *all* four "operations" in Figure 2:

1. In the "precharge operation": "The *precharge voltage Vpre*" is "applied between the drain and the source of the *drive transistor Tr13*" and "the *precharge current Ipre* of the large current . . . flows . . . between the drain and the source of the *drive transistor Tr13*." '615 at Fig. 3A, 20:22-2, 20:66-21:4; Kanicki Resp. Decl. ¶13.

2. In the "threshold correction operation": "*the drive transistor Tr13 is kept at the on state* by the electric charges . . . [t]herefore, the *current may flow between the drain and the source of the drive transistor Tr13*." '615 at Fig. 3B, 21:35-41; Kanicki Resp. Decl. ¶14.

3. In the "writing operation": "*gradation sequence current Idata* [flows] between the drain and the source of the *drive transistor Tr13*." '615 at Fig. 4A, 23:37-41; Kanicki Resp. Decl. ¶15.

4. In the "light emission operation": "*light emission drive current Iem flows* in the direction of the organic EL element OEL from the supplying voltage line VL via the *drive transistor Tr13*." '615 at Fig. 4B, 25:46-53; Kanicki Resp. Decl. ¶16.

Drive transistor Tr13 is also involved in performing the other "operations" identified in the specification. For example, the specification uses the term "drive control operation" to refer to the overall process shown in Figure 2, including all four "operations," and uses other terms, "display operation" and "gradation sequence display operation," to refer to all or parts of the overall process. '615 at 15:50-52, 27:9-15, 23:20-26. Given that the drive transistor Tr13 is involved in all four "operations" in Figure 2, it is necessarily involved in these overall "operations" as well.

Given the several different "operations" that the "light emission control section" performs, there is no basis for Solas's conclusion that "the operation" *must* refer to the 36-word phrase in its proposal or just the functions that another claim element attributes to the "light emission control

section." The uncertainty surrounding the meaning of "the operation" distinguishes the lone case *Solas* cites in its favor, *In re Downing*, 754 F. App'x 988, 996 (Fed. Cir. 2018). In that case, there was no antecedent basis for "the end user." *Id*. But the court found against indefiniteness because the specification explained that "end user" referred to "end user using the product," and there were no other plausible options for who "the end user" could be. *Id*. By contrast, there are several different "operations" in the specification that "the operation" could be referencing.

Moreover, in *In re Downing*, the meaning of "the end user" was apparent enough that the court did not need to correct or rewrite the claim to provide antecedent basis. No so here. Solas's proposal effectively requires replacing "the operation" with a 36-word phrase. Courts have refused to correct antecedent basis deficiencies if the correction addresses "more than a misspelling or a missing letter" or an "obvious clerical error." *Smith v. ORBCOMM, Inc*., No. 2:14–CV–666, 2015 WL 5302815, at *12 (E.D. Tex. Sept. 10, 2015); *Smartflash LLC v. Apple Inc.*, 77 F. Supp. 3d 535, 560-61 (E.D. Tex. 2014). Solas's insertion of 36 words far exceeds a minor correction.[6]

B. "precharge voltage" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
Plain and ordinary meaning	Indefinite

In its opening brief, Solas professes not to grasp the indefiniteness problem with "precharge voltage" and states that it will respond to HP's opening brief. Solas Open. Br. at 25-26. Accordingly, HP refers the Court to HP's opening brief and Dr. Kanicki's declaration for why "precharge voltage" is indefinite. Defs. Open. Br. at 19-21; Kanicki Op. Decl. ¶¶64-74.

[6] HP confirms Solas's understanding that HP is not contending that "the operation state" in Claim 11 is indefinite. *See* Solas Open. Br. at 25. "Operation state" is a separate noun from "operation" alone and the two are unrelated concepts. For that reason, "operation state" cannot provide antecedent basis for "the operation" and Solas does not contend otherwise in its opening brief. *Id*.

The little that Solas says in its brief only underscores the indefiniteness problem with "precharge voltage." Solas states: "the claim language teaches that the precharge voltage (a) exceeds a threshold value of the drive transistor, (b) is applied by the data driver to the data line, and (c) is applied by the light emission drive circuit to the electric charge accumulation section" via the writing control section. Solas Open. Br. at 26. As discussed in HP's brief, there is no single "precharge voltage" in the specification with *all three* characteristics recited in Claim 11. Instead, the specification describes *two* different types of "precharge voltages"—"Vpre" and "Vpre13"—depicted in Figure 3A (annotated), with each type including only *some* of the characteristics that Claim 11 attributes to its "precharge voltage," while excluding the others:

(1) The "precharge voltage" called "Vpre" (red) is applied by the data driver to the data line. But Vpre does *not* exceed the threshold value of the drive transistor (labeled "Vth13") and is *not* applied to the "electric charge accumulation section," which is the capacitor labeled Cs, via the writing control section (transistor Tr12).

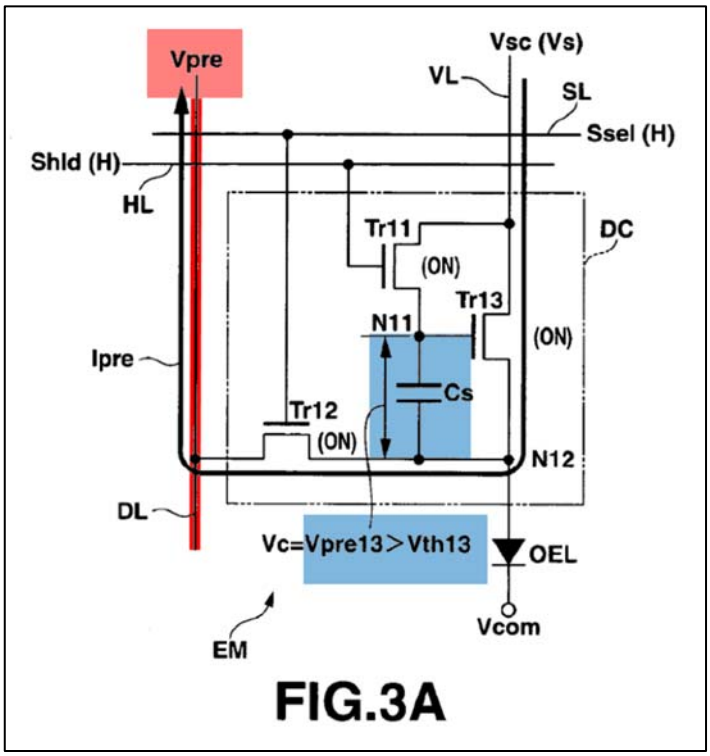


FIG.3A

(2) The "precharge voltage" called "Vpre13" (blue) exceeds the threshold value of the drive transistor Vth13 (as indicated by "Vpre13 > Vth" in Figure 3A). But Vpre13 is *not* applied by the data driver to the data line and *is not* applied to the "electric charge accumulation section [i.e., capacitor Cs]" "via

the writing control section" (transistor Tr12 in Figure 3A) as required by Claim 11. *See* Defs. Open. Br. at 19-21; Kanicki Op. Decl. ¶¶64-74.

The "precharge voltage" recited in Claim 11 is thus an amalgamation of two distinct "precharge voltages" (Vpre and Vpre13) in the specification. This amalgamation, however, is improper as it results in a new, fictitious "precharge voltage" that does not actually exist in the '615 Patent. Thus, Claim 11's "precharge voltage" is indefinite because a person of ordinary skill could not understand its scope or meaning with reasonable certainty based on the intrinsic record.

C. "writing control section" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
Plain and ordinary meaning, *i.e.*, circuit section that controls writing	"a transistor that controls the writing of both the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section"

Solas's proposal and opening brief arguments for "writing control section" are prime examples of its flawed approach of construing claims in a "vacuum" as the Federal Circuit has admonished. *Phillips*, 415 F.3d at 1313, 1320-21. Solas asserts, without support, that this term is "composed of ordinary technical words and has a plain meaning." Solas Open. Br. at 26-27. Based on this flawed assertion, Solas proposes a construction of "circuit section that controls writing" that simply rearranges the words in the term.

But "writing control section" is not a term with a plain meaning. Instead, like the other "sections" recited in Claim 11, "writing control section" is a phrase coined by the '615 Patent to refer to a specific structure with a specific function within the larger "light emission drive circuit" in Claim 11. The construction of "writing control section" must therefore reflect its structure and function as disclosed in the intrinsic evidence. *See Iridescent Networks, Inc. v. AT&T Mobility, LLC*, 933 F.3d 1345, 1353 (Fed. Cir. 2019) (finding that "because the disputed term is a coined

term . . . it has no ordinary and customary meaning," one must look at "the intrinsic evidence [to] provide[] objective boundaries to the scope of the term.").

As detailed in HP's opening brief, the '615 Patent specification uses an equivalent term, "writing control means," to refer to "selection transistor Tr12," shown in purple in annotated Figures 3A and 4A below. Defs. Open. Br. at 21-22; '615 at 17:7-9. As Figures 3A and 4A also show, the selection transistor Tr12 performs two functions: (1) applying a "precharge voltage" Vpre to a capacitor Cs (orange), also called the "charge accumulating section" ('615 at Fig. 3A, 20:36-43); and (2) applying a "gradation sequence current" Idata to the capacitor Cs (*id.* at Fig. 4A, 24:5-11). HP's construction of "writing control section" thus captures its structure ("a transistor") and function ("controls the writing of both the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section").

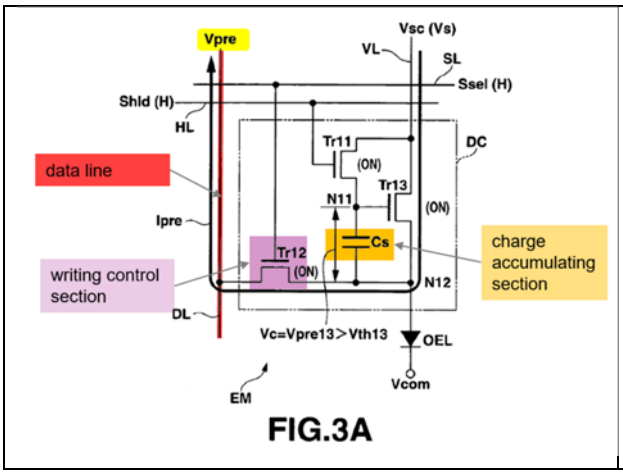


FIG.3A

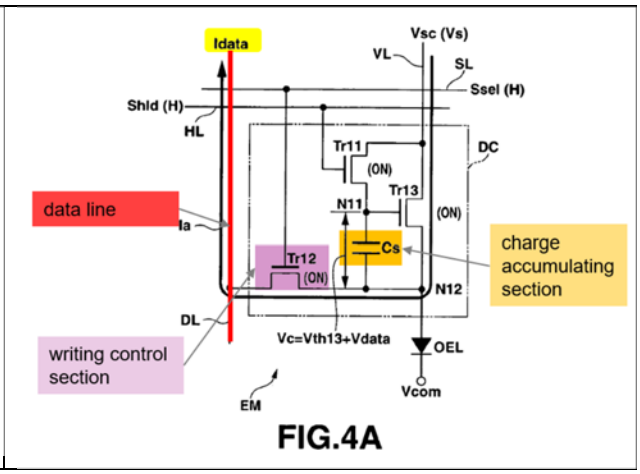


FIG.4A

Solas presents two criticisms of HP's construction, neither having merit. First, Solas contends that Claim 11 recites only one function for the "writing control section," which is writing "the *gradation sequence signal* to the electric charge accumulating section," and that HP's addition of another function of writing the "precharge voltage" is "manufactured." Solas Open. Br. at 27. But Solas ignores Claim 11's additional recitation that the "light emission drive circuit applies the precharge voltage applied to the data line to the electric charge accumulating section via the *writing*

control section." This recitation matches Figure 3A above and related text, which describes the second function of the "writing control section" (transistor Tr12), which is passing through and writing a "precharge voltage" from the "data line" (red) to the "charge accumulating section," which is capacitor Cs (orange).

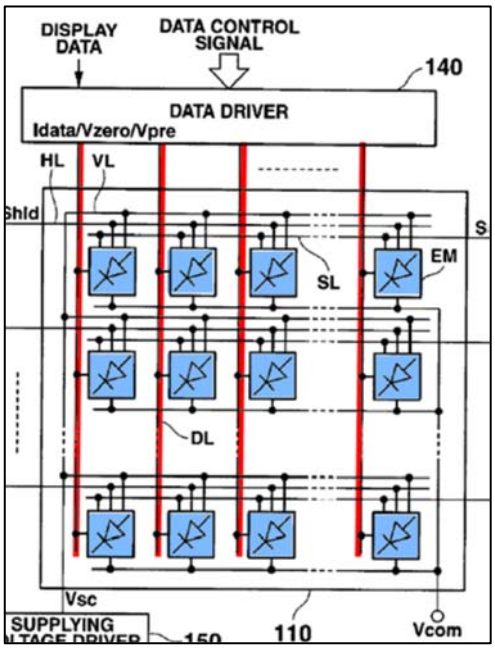
Second, Solas contends the patent does not "redefine or disclaim" the plain meaning of "writing control section" to limit it to "a transistor." Solas Open. Br. at 27. But as discussed, "writing control section" does not have a plain meaning that could be redefined or disclaimed; rather, it is a term coined and used by the '615 Patent to refer to a specific structure (i.e., selection transistor Tr12) within a pixel circuit as depicted in Figures 3A and 4A above. The doctrines of lexicography and disclaimer are therefore irrelevant to determining the term's meaning. At any rate, as discussed above, the '615 Patent equates a nearly identical term, "writing control means," with the selection transistor Tr12, stating: "[a]s shown in FIG. 1 . . . a light emission drive circuit DC according to the invention is configured so as to have: *a selection transistor (writing control means) Tr 12*." '615 at 17:7-9. Thus, the "writing control section" is "a transistor."

D. "data lines" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
Plain and ordinary meaning, i.e., conductive lines for supplying information	"conductive lines, each connected to and carrying data to a plurality of light emission drive circuits"

The parties' briefs present contrasting approaches for how to define "data lines." HP's construction follows from the context of the '615 Patent and OLED technologies. Defs. Open. Br. at 23-24. In both contexts, as depicted in annotated Figure 16 below, an OLED display panel comprises a grid of many pixels (blue) arranged across many rows and columns. The "data lines" (red) connect to the columns of pixels, where each individual "data line" connects to one column of pixels and each pixel includes a "light emission drive circuit." *Id.*

By contrast, Solas's brief admits that its construction follows from a single dictionary definition of an unrelated term, "data transmission line," as "[a] system of electrical conductors, such as a coaxial cable or pair of wires, used to send information from one place to another or one part of a system to another." Solas Open. Br. at 27; *id*. at Ex. 10 at 490 (underlining added). Moreover, Solas's brief conveniently omits the underlined portion of the definition (". . . such as coaxial cable or pair of wires . . ."), which reveals that the definition has no applicability to the '615 Patent and OLED circuits because "data lines" in such circuits are not coaxial cables or wire pairs.



Solas also fails to articulate any basis to reject the requirement that each "data line" connect to a "*plurality* of light emission drive circuits." Solas asserts that the requirement "is unsupported" and the "specification does not require" it. Solas Open. Br. at 28. Solas, however, cites nothing to support it assertion, and for good reason. In truth, *every* embodiment in the specification, including that of Figure 16, shows that each individual "data line" (red) connects to a column of multiple pixel circuits (blue), with each pixel circuit including a "light emission drive circuit." There is no contrary embodiment where each "data line" connects to *only one* single pixel circuit. *See Regents of Univ. of Minn.*, 717 F.3d at 935 (construing claims consistently with "every single embodiment" and because there was no contrary embodiment); *ICU Medical*, 558 F.3d at 1375-76 (same). Indeed, such a contrary embodiment would be absurd as it would require an OLED display panel having only one pixel or one row of pixels. Solas is thus incorrect in asserting that the "plain meaning" of "data lines" in the '615 Patent permits each line to connect to only one pixel.

Finally, Solas objects to HP's construction for using words "data" and "lines" that are in the disputed term. Solas Open. Br. at 28. Solas's objection is yet another example of Solas raising superficial criticisms to the form or wording of Defendants' construction in order to distract from the real, substantive differences between the parties. Solas's objection is also hypocritical. Several of Solas's own proposals simply rearrange the words in the term itself and are thus objectionable on the same grounds, including: "selection period" (Solas proposes "time *period* during which a plurality of pixel circuits is *selected*"); "designating current" (Solas proposes "*current designating* a value corresponding to an image signal"); "current lines" (Solas proposes "conductive *lines* for carrying *current*"); "writing control section" (Solas proposes "circuit *section* that *controls writing*"); and "signal lines" (Solas proposes "conductive *lines* supplying *signals*").

IV. U.S. Patent No. 7,573,068 ("'068 Patent")

A. "formed on said plurality of supply lines along said plurality of supply lines" (Claim 1) / "connected to said plurality of supply lines along said plurality of supply lines" (Claim 13)

Plaintiff	Defendants
"formed on said plurality of supply lines over the length or direction of said plurality of supply lines"	"stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line"
"connected to said plurality of supply lines over the length or direction of said plurality of supply lines"	

The '068 Patent discloses *only* two ways to "form" or "connect" the feed interconnections to the supply lines: (1) stacking the feed interconnection on top of the supply line over the length of the supply line (Figures 1 and 8), *or* (2) a grid formation in which the feed interconnections make multiple contacts with the plurality of supply lines over the length of each supply line (Figures 20 and 21). As Defendants detailed in their opening brief, their construction accounts for both the "stacked" embodiment ("stacked on . . . said plurality of supply lines over the length of each supply line") and the "grid" embodiment (". . . making multiple contacts with said plurality

of supply lines over the length of each supply line"). Defs. Open. Br. at 26-27. Solas's constructions go beyond the only two embodiments, encompassing an arrangement where the feed interconnections make only a *single* contact with each supply line. The '068 Patent does not enable any such embodiment and neither Solas nor its expert, Mr. Flasck, present any evidence from the '068 Patent to suggest otherwise.

In fact, Solas's brief avoids any discussion of intrinsic evidence, the two embodiments in the '068 Patent, or the core issue of whether the patent discloses or enables the "single contact" arrangement that Solas's constructions encompass. Instead, Solas focuses on extrinsic evidence, citing dictionary definitions of just one word, "along," in the 13-word disputed phrases. Solas Open. Br. at 14-15. The definitions that Solas cites, however, have no relevance to the parties' dispute. They shed no light on how feed interconnections are formed on or connected to supply lines. *Id.* Moreover, in discussing the definitions, Solas actually argues *against* its own construction, stating that: "[a] POSITA *would not* understand that interconnections are formed on or connected to the supply lines over the length or direction of the supply lines." Solas Open. Br. at 14 (emphasis added). Defendants agree—the phrase "over the length or direction of said plurality of supply lines" in Solas's construction is ambiguous and overbroad, and provides a POSITA with little guidance on how to form or connect feed interconnections and supply lines. Defs. Open. Br. at 27.

Unable to dispute the correctness of Defendants' construction, Solas resorts to misinterpreting it or making superficial objections about its word choice. First, Solas misinterprets Defendants' construction when it asserts "[n]othing in the claims require the interconnections to cover the entire length of or [*sic*] the supply lines." Solas Open. Br. at 14-15. Defendants' construction does not require that the interconnections must *cover* the *entire* length of the supply

lines—it permits the feed interconnections to "mak[e] multiple contacts" with each "supply line" as in the "grid" embodiment. Solas's constructions, by contrast, are flawed because they do not reflect that the '068 Patent requires sufficient contacts between the feed interconnections and supply lines to achieve the patent's objective of lowering the resistance of the supply lines. *See, e.g.*, '068 at 2:39-41, 4:4-14, 4:24-35; *see also* Solas Open. Br. at 4; Flasck Decl. ¶39. Indeed, Solas's expert has expressly admitted that having only a single contact between a supply line and a feed interconnection would not achieve the '068 Patent's objective because "you would expect a voltage drop and a signal delay." Defs. Open. Br., Ex. DD03 at 213:19-215:10. Thus, Solas's construction is improper. *Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1324 (Fed. Cir. 2008).

Second, Solas takes issue with Defendants' use of the phrases "stacked on" and "making multiple contacts with." Solas Open. Br. at 15. Solas argues that "'formed on' and 'connected to' have different meanings and it is thus improper to assign the same meaning to both." *Id*. But Solas fails to articulate any actual difference between the two phrases in the context of the '068 Patent, and identifies nothing to support that the '068 Patent treats the actions of "forming" or "connecting" a feed interconnection on or to a supply line differently. *Id*. Significantly, Mr. Flasck confirmed that there is no material difference between "formed on" and "connected to," stating that the two embodiments of the '068 Patent both "comport with the claim language in both claim 1 ['formed on'] and claim 13 ['connected to']." Flask Decl. ¶91.

Third, Solas's criticism of the phrases "stacked on" and "making multiple contacts with" ignores that they follow from the '068 Patent and are strikingly similar to language Mr. Flasck uses to describe the '068 Patent. The phrase "stacked on" quotes directly from the specification, '068 at 3:62-63, and is also clearly depicted in Figure 8. *See* Defs. Open. Br. at 25-26. In describing this embodiment, Mr. Flasck states that: "Fig 8 shows the feed interconnections [blue] formed *directly on the top surface of* the supply line Zi [red]." Flasck Decl. at ¶ 89 (emphasis added). The phrase "stacked on" in Defendants' construction is substantively identical to Mr. Flasck's language "formed directly on the top surface."

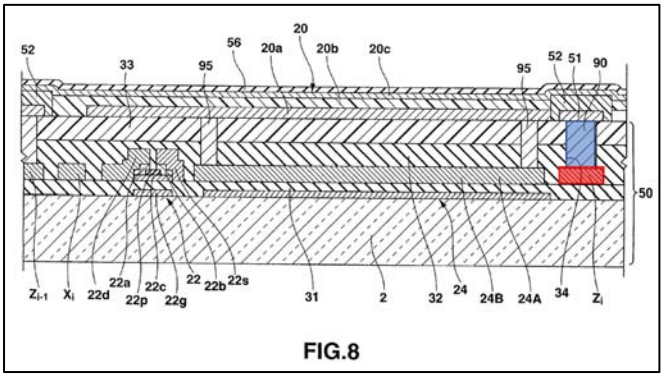
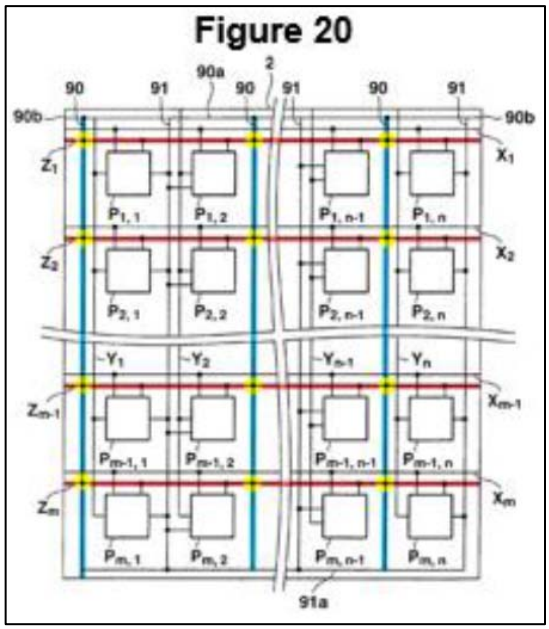


FIG.8

The same holds true for the phrase "making multiple contacts with." As discussed, Defendants' construction reflects the second "grid" embodiment in which the plurality of feed interconnects 90 (blue) running vertically in Figure 20, make multiple contacts (yellow) with the plurality of supply lines Zm (red) running horizontally. '068 at Fig. 20; *see also* Defs. Open. Br. at 26-27. Neither Solas nor Mr. Flasck dispute that "making multiple contacts with" is an accurate description of this embodiment. Nor could they given that Mr. Flasck describes Figure 20 using similar language: "each feed interconnection 90 *crosses and connects* to each supply line (Zi) at



the *crossovers* C2." Flasck Decl. at ¶90. Mr. Flasck's description—"crosses and connects . . . at the crossovers"—conveys the same concept as "multiple contacts" in Defendants' construction.

Fourth, Solas attacks Defendants' use of the word "each" in the phrase "over the length of *each* supply line." Solas Open. Br. at 15. But Solas again ignores that Mr. Flasck himself describes the "grid" embodiment in the very same way: "each feed interconnection 90 crosses and connects to *each* supply line (Zi)." Flasck Decl. at ¶90 (emphasis added). There is no merit to any of Solas's superficial attacks on Defendants' construction. Because only Defendants' construction accurately reflects the only two embodiments in the '068 Patent, it should be adopted.

B. "signal lines" / "supply lines" (Claims 1, 13)

Term	Plaintiff	Defendants
"signal lines"	"conductive lines supplying signals"	"conductive lines carrying data"
"supply lines"	"conductive lines supplying current or voltage"	"conductive lines, each supplying a driving current or voltage to a plurality of pixel circuits"

Solas's cursory discussion of "signal lines" and "supply lines" in separate sections of its brief fails to hide the flaw in its constructions: Solas's constructions erase any distinction between the two types of lines, making them interchangeable because in any circuit, every "signal" is represented as a "current or voltage." It is axiomatic that distinct terms are presumed to have different meanings. *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008). Solas does not contend that this presumption has been rebutted here. Solas Open. Br. at 13-16. Nor does Solas contend that there is any distinction between "signals" and "current or voltage" that could differentiate its constructions of "signal lines" and "supply lines." *Id.*

The '068 Patent confirms that the "signal lines" and "supply lines" have different functions and structures. Def. Open. Br. at 29-30 (citing '068 at 1:41-44, 15:61-63, 16:52-54). Each type of line carries a distinct type of current or voltage, and Defendants' constructions reflect this

difference. The supply lines supply a "driving current" that is a power supply. The specification teaches that "the *driving current* flows from the feed interconnection 90 and *supply line* Zi . . . to the organic EL element" and a "*driving current* having a magnitude corresponding to the level of the gate voltage *is supplied from the power supply*." '068 at 1:41-44, 16:52-54 (emphasis added). In other words, the "supply line" supplies a driving current to illuminate the pixel. Neither Solas nor its expert dispute this.[7]

Solas nonetheless opposes Defendants' construction of "supply lines" by pointing to a portion of the specification stating that a "supply line" can *also* supply a "write current." Solas Open. Br. at 14 (citing '068 at 16:17-21, 16:52-55, 19:26-30). This is a red herring. Nowhere does Defendants' construction state, or even imply, that "supply lines" can supply *only* a "driving current." That supply lines can *also* supply a write current does not change the fact that the '068 Patent explicitly teaches that only the "supply lines" provide a "driving current" to pixel circuits. *See, e.g.,* '068 at 16:38-61, Figs. 1, 20; Def. Open. Br. at 29-30. In the '068 Patent, no lines other than the "supply lines" can supply a "driving current" to the pixel circuits. By recognizing the unique function of "supply lines" in supplying a "driving current," Defendants' construction properly reflects the intrinsic evidence and distinguishes "supply lines" from "signal lines."

Solas also takes issue with the phrase "to a plurality of pixel circuits" in Defendants' construction, arguing that "there is no necessary one-to-many relationship between each supply line and a plurality of pixel circuits." Solas Open. Br. at 13. But Solas does not, and cannot, show a single instance in which the '068 Patent discloses and enables a single supply line feeding only

[7] Solas's statements elsewhere in its brief support Defendants' construction of "supply lines." In its discussion of the '338 Patent, which shares several inventors and a portion of the specification with the '068 Patent, Solas specifically describes current supplied by a supply line to a pixel circuit as a "driving current": "[d]uring the time that the sub-pixel is emitting light, a 'driving current' passes through the driving transistor and is supplied to the diode." Solas Open. Br. at 3.

a single pixel circuit. Every disclosure of the '068 Patent teaches that each supply line "Z_m" provides a driving current or voltage to *multiple* pixel circuits, as Defendants' construction reflects. *See, e.g.,* '068 at 16:38-61, Figs. 1, 20; Def. Open. Br. at 29-30. *See Regents of Univ. of Minn.*, 717 F.3d at 935-36 (construing claims consistently with "every single embodiment" and because there was no contrary embodiment); *ICU Medical*, 558 F.3d at 1375-76 (same). Thus, Solas's attempt to broaden the construction of "supply lines" to encompass a single line supplying only a single pixel circuit should be rejected.

Solas's argument regarding "signal lines" is equally flawed. Solas, in fact, admits that the '068 Patent "describes conductive lines that supply signals where the signals can be currents or voltages." Solas Open. Br. at 15-16. Solas's statement highlights the flaw in its constructions: a signal is represented by a current or voltage, and accordingly, there is *no distinction* between Solas's constructions of "supply lines" ("conductive lines supplying current or voltage") and "signal lines" ("conductive lines supplying signals [*i.e.,* currents or voltages]"). These are different terms with a presumption of different meanings. *Helmsderfer*, 527 F.3d at 1382. Defendants' construction correctly reflects that data is carried on the signal line, as the intrinsic evidence discloses: "a *data* driver supplies a *write current* (current signal) to all the *signal lines* Y1 to Yn." '068 at 15:61-63 (emphasis added); Def. Open. Br. at 29. "Supply lines" and "signal lines" are not the same lines, and Defendants' constructions accurately reflect these differences.

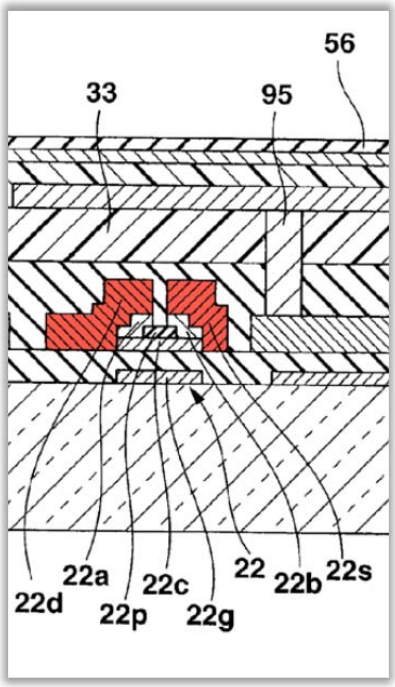
C. "source" / "drain" (Claims 1, 13)

Plaintiff	Defendants
Plain and ordinary meaning	"source electrode" / "drain electrode" Alternatively: "the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region."

Solas's brief underscores why plain and ordinary meaning is inadequate here—the plain and ordinary meaning provides no guidance as to what structures within a thin film transistor (TFT)

a "source" and "drain" encompass in the context of the '068 Patent. For example, if "source" and "drain" are left unconstrued, it will be unclear if they refer to conductive structures, semiconductor regions, insulating layers, or something else in a TFT. In contrast, Defendants' constructions identify with particularity the portions of the TFT that the '068 Patent consistently and exclusively refers to as "source" or "drain": the patterned "conductive film," commonly referred to as an "electrode,"[8] formed on top of and separately from the "impurity-doped semiconductor film." Def. Open. Br. at 31 (citing '068 at 8:64-66, 9:36-44).

In fact, despite Solas's one paragraph of cursory objections to Defendants' constructions, the six paragraphs of opinions from its expert Mr. Flasck demonstrate complete agreement with Defendants as to the meaning of "source" and "drain" in the context of the '068 Patent. Solas Open. Br. at 16; Flasck Decl. ¶¶97-102. In considering the same Figure 5 (excerpted with Mr. Flasck's red annotations) and specification passages as those discussed in Defendants' opening brief, Mr. Flasck agrees that the "source" and "drain" are elements 23s and 23d (both red), respectively, in Figure 5. *Compare id*. at ¶¶98-99, *with* Defs. Open. Br. at 31. In further agreement with Defendants' opening brief, Mr. Flasck explains that elements 23s and 23d are



[8] "Electrode" is often used as shorthand for conductive structures. *See, e.g.,* Ex. DD07 at 237 ("A *conductor* which serves to deliver, receive, collect, emit, deflect, or control electric charge carriers. An electrode provides the path for current entering or leaving a medium such as a dielectric, electrolytic solution, semiconductor, gas, or vacuum."); Ex. DD08 at 139 ("a *conductor* in an electronic device that is at some ELECTRIC POTENTIAL and which can collect or emit charged particles."); Ex. DD09 at 545 ("a *conductor* through which electricity enters or leaves an object, substance, or region.").

formed from "conductive films" formed on top of elements 23a and 23b, which are distinct and formed from a separate "impurity-doped semiconductor film." *Id*.

Based on these disclosures, Mr. Flasck defines "source" and "drain," stating: "a POSITA would know that the source (or drain) is *the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region*." Flasck Decl. ¶101; *see also id*. at ¶100 ("in the '068 patent, the source and drain comprise patterned conductive films that connect the TFT channel ends to other circuit elements").

Although Solas and Mr. Flasck agree that "source" and "drain" refer to patterned conductive film structures, they object to Defendants' use of the word "electrode" as shorthand for such patterned conductive film structures. Solas Open. Br. at 16; Flasck Decl. ¶¶100-101. Mr. Flasck claims that the meaning of "electrode" is ambiguous,[9] opining that his own definitions of "source" and "drain" are more precise and specific to the context of the '068 Patent. Flasck Decl. ¶¶100-101. While Defendants disagree (*see* n. 8, *supra*), in an effort to eliminate any dispute, Defendants propose an alternative construction of "source" and "drain" that adopts Mr. Flasck's definition of those terms: "the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region." *Id*. at ¶101.

[9] Solas's and Mr. Flasck's objections to "electrode" as ambiguous are curious given that Mr. Flasck explains that "gate electrode" is "easily understood because indeed the gate is a metal conductive film, so the use of 'gate electrode' is routine." Flasck Decl. ¶97. If "gate electrode" is a "routine" and "easily understood" reference to the "conductive film" that forms the gate, it is unclear why the same would not hold true for "source electrode" and "drain electrode."

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document on July 16, 2020.

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